

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Shigeru ATSUMI

Serial No. 09/028,276

Filed: February 24, 1998

For: SEMICONDUCTOR INTEGRATED
CIRCUIT DEVICE AND FLASH
EEPROM



Group Art Unit: 2815

Examiner: Jesse A. Fenty

Atty Dkt No. 1701.73982

*18/ Appeal
Brief
J. Steptae
10/24/00*

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APPEAL BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This is a brief in accordance with 37 C.F.R. §1.192, filed in support of Appellant's August 17, 2000, Notice of Appeal. A check in the amount of \$310.00 is attached to cover the Appeal Brief fee specified in 37 C.F.R. §1.17(c). In the event any variance exists between the amount enclosed and the Patent Office fees, please charge or credit any difference to our Deposit Account No. 19-0733.

I. REAL PARTY IN INTEREST

The owner of this application, and real party in interest, is Kabushiki Kaisha Toshiba Corporation.

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GP 2815

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Atty. Docket: 1701.73982

APPEAL BRIEF TRANSMITTAL

Commissioner of Patents
Washington, D.C. 20231

Sir:

Appellants transmit herewith in triplicate their Brief on Appeal.

- ☒ Appeal Brief Fee\$310.00
- ☐ Appellants petition for an extension of
time for the minimum period needed for the
timely filing of this Appeal Brief, which
is calculated as being * (*) months0.00
- ☒ Our check is included for the amount in total\$310.00

In the event an insufficient time or fee is calculated, or if our check should be detached herefrom, appellants petition for the grant of the minimum extension of time needed to effect the timely filing of this Appeal Brief and/or authorize the payment of any fee needed from our Deposit Account No. 19-0733. In the event of overpayment, it is requested such overpayment be credited to our Deposit Account No. 19-0733.

Respectfully submitted,

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Date: October 17, 2000

JMP/AKM/daw

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II. RELATED APPEALS AND INTERFERENCES

There are no appeals nor interferences related to the present appeal.

III. STATUS OF CLAIMS

Claims 1-42 remain pending. The final Office Action, mailed May 17, 2000 (Paper No. 16), rejected claims 1, 2 and 21-26 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,471,373 to Shimizu et al. (Shimizu) and claims 3-9, 13, 14, and 27-42 under 35 U.S.C. §103(a) as being obvious over Shimizu. That Office Action also objected to the drawings under 37 C.F.R. §1.83(a). The rejections of claims 1, 2 and 21-26 under 35 U.S.C. §102(b); the rejections of claims 3-9, 13, 14, and 27-42 under 35 U.S.C. §103(a) and the objection to the drawings under 37 C.F.R. §1.83(a) are appealed.

Claims 10-12 and 15-20, which were subject to an election of species requirement made in the Office Action mailed on December 7, 1998 (Paper No. 4), were withdrawn from consideration in the Office Action mailed January 28, 1999 (Paper No. 6), but may be reconsidered upon allowance of a generic claim under 37 C.F.R. §1.141. The election of species requirement is not appealed.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final Office Action.

V. SUMMARY OF INVENTION

The specification is directed generally to a semiconductor substrate including multiple transistors formed on the substrate and having different gate insulation film thicknesses. Transistors having a thicker film thickness are connected directly to external terminals, such as input/output terminals and a power supply terminals, and transistors having a thinner film thickness are not directly connected to external terminals.

Fig. 7 shows a semiconductor substrate having a plurality of external terminals 2 (e.g., input/output terminals 23 and power supply terminal 21) connected to internal circuit 4, such as a memory array cell, via interface circuits 3. Interface circuits 3 having MOS transistors connected directly to the power supply terminal 21 and input/output terminals 23 are made of transistors, shown in Fig. 2B, having thick gate oxide films. Interface circuits 3, having MOS transistors not connected directly to an external terminal, are made of transistors, shown in Fig. 2A, having thinner gate oxide films. *See specification, page 15, lines 6-19.* Fig. 8 depicts an interface circuit 3 having thick gate oxide film transistors P1 and P2 connected directly to a power supply voltage. *See specification, page 16, lines 5-22.* PMOS transistor P5 connected to output terminal TMout is also a thick gate oxide film transistor. Transistors, such as transistors constituting inverter INV are not directly connected to external terminals and are made of thin gate oxide film transistors. *See specification, page 16, line 23-page 17, line 20.*

Conventionally, transistors formed on a semiconductor device include gate oxide films of the same thickness. This structure gives rise to a variety of problems in semiconductor devices, such as

memory devices, that utilize a wide range of voltages. Generally, transistors formed on these semiconductor devices have thick gate oxide films for accommodating the higher voltages in the range, *e.g.*, 10 V. Thick gate oxide films allow transistors to withstand high voltages that would otherwise cause a thinner gate oxide film to breakdown. However, using only thick gate oxide transistors limits the number of transistors that may be formed on a semiconductor device, and causes deterioration in the transistors' characteristics. *See* specification, page 3, lines 2-23. Therefore, including multiple transistors formed on the substrate and having different gate insulation film thicknesses according to the present invention increases the number of transistors that can be formed on a semiconductor device.

Separate summaries for each of the invention groups set forth in Section VII, *infra*, are set forth below.

A. Group I (claims 1, 4, 21, 24, 32 and 35)

Independent claims 1, 21 and 32 and dependent claims 4, 24 and 35 recite that a semiconductor substrate including a plurality of transistors is formed on the substrate, and the plurality of transistors have different gate insulation film thicknesses. A transistor connected directly to an input/output terminal on the semiconductor substrate is one of the transistors other than a transistor having the thinnest gate insulation film.

The elements of claims 1, 4, 21, 24, 32 and 35 are clearly set forth in the text and drawings of the specification. Fig. 8 shows transistors P5 and N5 always physically connected directly to an output terminal TMout, absent any intervening elements. *See* specification page 17, line 21-page 18,

line 8. Fig. 9 shows transistors P6 and N6 always physically connected directly to an input terminal TMin, absent any intervening elements. Transistors P5, P6, N5 and N6 are thick gate oxide transistors, instead of thin gate oxide transistors used for the inverters. *See* specification page 18, lines 8-21.

Appellant has recognized an advantage with the structures recited in independent claims 1, 21 and 32 in that a plurality of transistors based on gate oxide films of two or more different thicknesses can be integrated within one chip without deterioration in the transistor characteristics. Also, by using thicker gate oxide films for transistors directly connected to input/output terminals, electrostatic discharge is reduced and breakdown voltage is increased. Therefore, the transistors directly connected to external terminals, which are subject to higher voltages than transistors not directly connected to external terminals, can withstand high voltages without deteriorating.

B. Group II (claims 2, 3, 5, 6, 22, 23, 25, 26, 33, 34, 36 and 37)

Claims 2, 5, 22, 25, 33 and 36 generally recite, *inter alia*,

a power supply terminal to which an external power supply voltage is applied, wherein a transistor connected directly to the power supply terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

Claim 3, 6, 23, 26, 34 and 37 generally recite, *inter alia*:

wherein a transistor having a current path connected between the power supply terminal and the ground terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

Fig. 8 shows thick gate oxide transistors P1-P5 connected directly to the power supply voltage and/or having a current path connected between a power supply terminal and a ground terminal. *See* specification, page 16, lines 7-9; page 17, lines 9-20. These transistors are subject to higher voltages than transistors not directly connected to a voltage source. Therefore, transistors connected directly to the power supply voltage and/or having a current path connected between a power supply terminal and a ground terminal have a thicker gate oxide film that can withstand high voltages without deteriorating.

C. Group III (claims 7, 8, 27, 28, 38 and 39)

Claims 7, 27 and 38 recite an interface circuit including an input buffer circuit. An input buffer circuit is shown in Fig. 9. *See* specification page 18, lines 10-21. The input buffer circuit includes thick gate oxide transistors P6 and N6 connected directly to the power supply voltage and an input terminal TMin.

Claims 8, 28 and 39 recite an interface circuit including an output buffer circuit. An output buffer circuit is shown in Fig. 10. *See* specification page 18, line 22-page 18, line 9. The output buffer circuit includes thick gate oxide transistors P7 and N7 connected directly to the power supply voltage and an output terminal TMout. The structures of the input and output buffer circuits are effective for reducing electrostatic discharge and preventing deterioration of transistor oxide films.

D. Group IV (claims 9, 13, 14, 29-31 and 40-42)

Claims 9, 29 and 40 recite an interface circuit including a level shifter and an output buffer circuit.

Claims 13, 30 and 41 recite that the level shifter circuit converts a lowered potential signal obtained from a regulator circuit to a power supply voltage level.

Claims 14, 31 and 42 recite, "... a transistor included in the level shifter and a device directly receiving the lowered potential level signal is the transistor having the thinnest gate insulation film."

Fig. 8 shows an embodiment including level shifter 12 connected to output buffer 13. Level shifter 12 shifts voltages received from a regulator circuit, shown in Fig. 12, to the level of the power supply voltage and applies the voltage to the output terminal TMout via output buffer 13. *See* specification, page 16, lines 1-4; p. 17, lines 21-24. Transistors P1-P5 are thick gate oxide film transistors that can withstand the voltage level of the power supply without deteriorating. Devices, such as the inverter in level shifter 12, include thin gate oxide film transistors, because these transistors are subject to lower voltages. *See* specification, page 17, lines 17-20. Therefore, a semiconductor device including the claimed level shifter circuit and regulator circuit can accommodate transistors having different gate insulation film thicknesses.

VI. ISSUES

1. Whether claims 1, 2 and 21-26 are unpatentable under 35 U.S.C. §102(b) as being anticipated by Shimizu.

2. Whether claims 3-9, 13, 14, and 27-42 are unpatentable under 35 U.S.C. §103(a) as being obvious over Shimizu.

3. Whether the drawings, objected to under 37 C.F.R. §1.83(a), show a transistor connected to the input/output terminal absent any intervening elements.

VII. GROUPING OF CLAIMS

In accordance with 37 C.F.R. §1.192(c)(7), Appellant respectfully requests that the claims not stand or fall together. Appellant requests that the following groups of separately patentable claims be recognized:

GROUP I -- Independent claims 1, 21 and 32 and claims 4, 24 and 35;

GROUP II -- Claims 2, 3, 5, 6, 22, 23, 25, 26, 33, 34, 36 and 37;

GROUP III -- Claims 7, 8, 27, 28, 38 and 39; and

GROUP IV -- Claims 9, 13, 14, 29-31 and 40-42.

In accordance with 37 C.F.R. §1.192(c)(7) - (8), separate arguments for patentability for Groups I-IV are provided in Section VIII, *infra*.

VIII. ARGUMENT

Claims 1, 2 and 21-26 stand rejected under 35 U.S.C. §102(b) as being anticipated by Shimizu. With respect to claims 1 and 21-26, the final Office Action alleges that Shimizu discloses a plurality of transistors, such as Q1, Q2, QE1, QE2, QE3, including gate insulation films of different thicknesses, an input/output terminal (5), and that a transistor QE2 physically connected directly to

input/output terminal (5), absent any intervening elements, is one of the transistors other than a transistor having the thinnest gate insulation film.

With respect to claim 2, the final Office Action alleges Shimizu discloses a power supply terminal (5), and that a transistor (QE3) connected directly to the power supply terminal is a transistor other than the transistors having the thinnest gate insulation film.

Claims 3-9, 13-14 and 27-42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimizu. With respect to claims 3-9, 13-14 and 27-42, the final Office Action alleges that Shimizu discloses the devices of claims 1 and 24 including a memory array, a decoder portion, an input/output circuit, thick gate oxide film transistors, terminals for external connections, use of thin gate oxide film transistors for a 'read' operation of an EPROM and use of thick gate oxide film transistors for a 'write' operation. The final Office Action admits that Shimizu does not expressly teach a ground terminal connected to a power supply terminal, a regulator circuit and a level shifter circuit including a transistor having the thinnest gate insulation film and receiving a lower level signal. However, the final Office Action alleges, absent any teachings, that it would have been obvious to one of ordinary skill in the art at the time the invention was made to couple a power supply line to a ground line and to construct "in between circuits" for the purpose of creating a buffer between the low and high voltage regions of a circuit.

A. Arguments With Respect To The Claims In Group I (independent claims 1, 21 and 32 and claims 4, 24 and 35)

Independent claims 1 and 21 and claims 4 and 24, dependent on claims 1 and 21 respectively, stand rejected under 35 U.S.C. §102(b) as being anticipated by Shimizu. Independent claim 1 recites, *inter alia*, a semiconductor integrated circuit device comprising:

a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed; and ...
a transistor physically connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

Independent claim 21 recites, *inter alia*, a semiconductor integrated circuit device comprising:

a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed; and ...
a transistor connected directly to the input/output terminal, absent any intervening elements, is one of the transistors other than a transistor having the thinnest gate insulation film.

The rejection of claims 1 and 21 allege that the claimed input/output terminal is met by the input/output terminal (5) disclosed by Shimizu, and a transistor physically connected directly to the input/output terminal (5), absent any intervening elements, and being one of the transistors other than a transistor having the thinnest gate insulation film is met by transistor (QE2) disclosed by Shimizu. Also, in the Response to Arguments section, the final Office Action alleges,

Shimizu (Column 6, lines 66-68; column 7, lines 1-3) describe an interconnect layer for connecting the transistors having the thicker gate oxide thickness. The description in column 1 explains how the integrated circuit is connected and one skilled in the art will know that the thick gate oxide transistors of the peripheral circuits (4) are physically directly connected to the input/output (Read/write) terminals (5). Shimizu does not disclose any intervening elements between these two regions. Those skilled in the art would know that an aluminum layer (31) for example as disclosed by Shimizu (Fig. 18) is a common and many times necessary component in device fabrication.

According to FIG. 18 and the corresponding description at column 6, line 66 to column 7, line 10 of Shimizu, the transistor QE2 is used for the writing operation, and is connected with an aluminum interconnection layer 31. **However, the specification is devoid of a teaching as to how the transistor QE2 or the interconnection layer 31 is connected to the input/output terminal 5 directly or otherwise.** Consequently, Shimizu lacks a teaching or suggestion that the transistor QE2 is *physically connected directly* to the input/output terminal 5, as called for in claim 1, and that the transistor QE2 is connected directly to the input/output terminal 5, *absent any intervening elements*, as called for in claim 21.

Appellant also submits that such teachings are not inherent from Shimizu. In the Response to Arguments section, the final Office Action appears to allege that inherently the aluminum interconnect layer 31 physically directly connects QE2 to input/output terminals (5). That the transistor may be connected in such a manner is not sufficient to establish inherency. It must necessarily be connected in such a manner. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Significantly, Appellant has recognized an advantage with the structures recited in claims 1 and 21 in

that a plurality of transistors based on gate oxide films of two or more different thicknesses can be integrated within one chip without deterioration in the transistor characteristics, and the breakdown voltage against electrostatic discharge can be reduced.

For anticipation under 35 U.S.C. §102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. *See* M.P.E.P., §706.02 Rejection on Prior Art. As stated above, Shimizu fails to teach every aspect of the invention as claimed in independent claims 1 and 21. Thus, claims 1 and 21 have been improperly rejected under 35 U.S.C. §102 as being anticipated by Shimizu.

Claims 4 and 24, which depend from claims 1 and 21 respectively, have also been improperly rejected under 35 U.S.C. §102 as being anticipated by Shimizu for at least the same reasons as claims 1 and 21. Additionally, Appellant submits that none of the features recited in claims 4 and 24 are taught either explicitly or impliedly by Shimizu. Specifically claims 4 and 24 recite, *inter alia*, "a transistor connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film." This feature is not taught by Shimizu for at least the reasons discussed above with respect to claims 1 and 21.

Independent claim 32 and claim 35, dependent on claim 32, stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimizu. Claim 32 recites, *inter alia*, a semiconductor integrated circuit device comprising:

a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed;
and ...

a transistor always connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

Independent claim 32 calls for, among other features, that a transistor *always connected directly* to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film. Apparently, the action recognizes that Shimizu does not teach or suggest all the features recited in claim 32, because this claim has been rejected as being obvious. In this regard, Appellant notes that the only difference between claim 32 and claim 1 is that claim 32 uses the word *always* rather than “physically” to describe the direct connection between the transistor and the input/output terminal. Therefore, the final Office Action inherently agrees that Shimizu fails to teach or suggest that a transistor *always connected directly* to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film. Additionally, Shimizu discloses a gate oxide transistor (e.g., QE2) is connected to the input/output terminal 5 during a write operation **and not necessarily connected during a read operation**. See Shimizu at column 7, lines 7-8. Furthermore, the final Office Action alleges, “Shimizu discloses the use of thin gate oxide transistors for the ‘read’ operation of an EPROM device and thick gate oxide transistors used for the ‘write’ operation, as well as other peripheral circuits.” This allegation in conjunction with the final Office Action’s inherent agreement (i.e., Shimizu fails to teach or suggest that a transistor *always connected directly* to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film) supports a conclusion that thick gate oxide transistors used for the ‘write’ operation in Shimizu are connected during the ‘write’ operation and not necessarily connected

during the 'read' operation. Therefore, the final Office Action acknowledges that Shimizu fails to teach or suggest that a transistor *always connected directly* to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film as required by claim 32. Also, the final Office Action fails to overcome this deficiency and identify any suggestion in Shimizu to modify the transistor QE2 to be *always* connected to the input/output terminal 5.

To establish *prima facie* obviousness, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); M.P.E.P. §2143.03. Since not all of the features in claim 32 are taught or suggested by Shimizu, it is clear that claim 32 cannot properly be rejected over Shimizu.

Claim 35, which depends from claim 32, has also been improperly rejected under 35 U.S.C. §103 as being obvious over Shimizu for at least the same reasons as claim 32. Additionally, Appellant submits that none of the features recited in claim 35 are taught or suggested by Shimizu. Specifically claim 35 recites, *inter alia*, "a transistor connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film." This feature is not taught or suggested by Shimizu for at least the reasons discussed above with respect to claims 1, 21 and 32.

B. Arguments With Respect To The Claims In Group II (claims 2, 3, 5, 6, 22, 23, 25, 26, 33, 34, 36 and 37)

Claim 2, dependent on claim 1, and claims 22, 23, 25 and 26, ultimately dependent on claim 21, stand rejected under 35 U.S.C. §102(b) as being anticipated by Shimizu. Claims 2, 22, 23, 25

and 26 have also been improperly rejected under 35 U.S.C. §102 as being anticipated by Shimizu for at least the same reasons as claims 1 and 21. Additionally, Appellant submits that none of the features recited in each of dependent claims 2, 22, 23, 25 and 26 are taught either explicitly or impliedly by Shimizu. Claims 2 and 22 recite, *inter alia*,

a power supply terminal to which an external power supply voltage is applied, wherein a transistor connected directly to the power supply terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

Claims 25 recites, *inter alia*,

a transistor ... connected directly to the power supply terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

Claims 23 and 26 recite that a transistor having a current path connected between the power supply terminal and the ground terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

Shimizu fails to teach or suggest that a transistor, other than a transistor having the thinnest gate insulation film, is connected directly to the power supply terminal, or that a transistor having a current path connected between the power supply terminal and the ground terminal is one of the transistors other than a transistor having the thinnest gate insulation film. Directly connecting a transistor, other than a transistor having the thinnest gate insulation film, to a power supply terminal is imperative for preventing the transistor from deteriorating due to the voltage from the power supply.

Claims 3, 5, 6, 33, 34, 36 and 37 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimizu. Appellant submits that claims 3, 5 and 6, which ultimately depend from independent claim 1, and claims 33, 34, 36 and 37, which ultimately depend from independent claim 32, have also been improperly rejected under 35 U.S.C. §103 as being obvious over Shimizu for at least the same reasons as claims 1 and 32. Additionally, Appellant submits that Shimizu fails to teach or suggest all of the features recited in each of dependent claims 3, 5, 6, 33, 34, 36 and 37.

Claims 5, 33 and 36 recite features similar to claims 2 and 22, and claims 3, 6, 34 and 37 recite features similar to claims 23 and 26. Shimizu fails to teach or suggest the features recited in claims 3, 5, 6, 33, 34, 36 and 37, as discussed above with respect to claims 2, 22, 23 and 26.

C. Arguments With Respect To The Claims in Group III (claims 7, 8, 27, 28, 38 and 39)

Claims 7, 8, 27, 28, 38 and 39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimizu. Appellant submits that claims 7 and 8, which ultimately depend from independent claim 1, claims 27 and 28, which ultimately depend from independent claim 21, and claims 38 and 39, which ultimately depend from independent claim 32, have also been improperly rejected under 35 U.S.C. §103 as being obvious over Shimizu for at least the same reasons as claims 1, 21 and 32. Additionally, Appellant submits Shimizu fails to teach or suggest all of the features recited in each of dependent claims 7, 8, 27, 28, 38 and 39.

Claims 7, 27 and 38 recite an interface circuit including an input buffer circuit. Claims 8, 28 and 39 recite an interface circuit including an output buffer circuit. The final Office Action alleges

that it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct "in between circuits" for the purpose of creating a buffer between the low and high voltage regions of a circuit. However, the final Office Action fails to cite a reference that teaches the claimed buffer circuits. It is respectfully submitted that the basis of the rejection is nothing more than an impermissible hindsight modification to Shimizu, absent a teaching of the claimed features not taught or suggested by Shimizu, using Appellant's claims as a guide.

D. Arguments With Respect To The Claims in Group IV (claims 9, 13, 14, 29-31 and 40-42)

Claims 9, 13, 14, 29-31 and 40-42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Shimizu. Appellant submits that claims 9, 13 and 14, which ultimately depend from independent claim 1, claims 29-31, which ultimately depend from independent claim 21 and claims 40-42, which ultimately depend from independent claim 32, have also been improperly rejected under 35 U.S.C. §103 as being obvious over Shimizu for at least the same reasons as claims 1, 21 and 32. Additionally, Appellant submits Shimizu fails to teach or suggest all of the features recited in each of dependent claims 9, 13, 14, 29-31 and 40-42.

Claims 9, 29 and 40 recite an interface circuit including a level shifter and an output buffer circuit.

Claims 13, 30 and 41 recite that the level shifter circuit converts a lowered potential signal obtained from a regulator circuit to a power supply voltage level.

Claims 14, 31 and 42 recite that a transistor included in the level shifter and a device directly receiving the lowered potential level signal is the transistor having the thinnest gate insulation film.

Shimizu fails to teach or suggest any of these features, and the rejection of claims 9, 13, 14, 29-31 and 40-42 in the final Office Action admits that Shimizu fails to expressly disclose a level shifter and regulator circuit. The rejection states that it would have been obvious to one of ordinary skill in the art to construct "other in between circuits" in Shimizu. However, the rejection fails to cite a reference that teaches the claimed features. It is respectfully submitted that the basis of the rejection is nothing more than an impermissible hindsight modification to Shimizu, absent a teaching of the claimed features not taught or suggested by Shimizu, using Appellant's claims as a guide.

E. The Drawings Are Improperly Objected To Under 37 C.F.R. §1.83(a)

The drawings stand objected to under 37 C.F.R. §1.83(a) for not showing the transistor connected to the input/output terminal absent any intervening elements.

Appellant submits that at least Figs. 7 and 8 show a transistor connected to the input/output terminal, absent any intervening elements. Fig. 7 shows interface circuit 3, including thick gate oxide transistors connected directly to input/output terminal 23, absent any intervening elements. Also, the specification, referring to Fig. 7, describes thick gate oxide transistors, as shown in Fig. 2B, connected directly to input/output terminal 23. *See* specification, page 15, lines 6-19. Also, Fig. 8 depicts thick gate oxide film transistor P5 directly connected to output terminal TMout, absent any intervening elements, and Fig. 9 depicts thick gate oxide film transistor P6 directly connected to

input terminal TMin, absent any intervening elements. *See* specification, page 17, lines 1-8; page 18, lines 8-21.

It is clear that the specification describes and at least Figs. 7-9 show a transistor physically connected directly to an input/output terminal, absent any intervening elements. Accordingly, the objection to the drawings cannot be properly sustained.

IX. CONCLUSION

For all of the foregoing reasons, the final rejection of claims 1, 2 and 21-26 under 35 U.S.C. §102(b); the rejections of claims 3-9, 13, 14, and 27-42 under 35 U.S.C. §103(a) and the objection to the drawings under 37 C.F.R. §1.83(a) are improper and should be reversed.

Respectfully submitted,

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Dated: October 17, 2000

APPENDIX

CLAIMS INVOLVED IN THE APPEAL

1. A semiconductor integrated circuit device comprising:

a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed; and

an input/output terminal formed on the semiconductor substrate, wherein a transistor physically connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

2. A semiconductor integrated circuit device according to claim 1, further comprising a power supply terminal to which an external power supply voltage is applied, wherein a transistor connected directly to the power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

3. A semiconductor integrated circuit device according to claim 1, further comprising a power supply terminal to which an external power supply voltage is applied and a ground terminal, wherein a transistor having a current path connected between the power supply terminal and the ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

4. A semiconductor integrated circuit device according to claim 1, further comprising an interface circuit connected to the input/output terminal, wherein a transistor included in the interface circuit and connected directly to the input/output terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

5. A semiconductor integrated circuit device according to claim 4, wherein a transistor included in the interface circuit and connected directly to a power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

6. A semiconductor integrated circuit device according to claim 5, wherein a transistor included in the interface circuit and having a current path connected between the power supply terminal and a ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

7. A semiconductor integrated circuit device according to claim 4, wherein said interface circuit includes an input buffer circuit.

8. A semiconductor integrated circuit device according to claim 4, wherein said interface circuit includes an output buffer circuit.

9. A semiconductor integrated circuit device according to claim 4, wherein said interface circuit includes a level shifter and an output buffer circuit.

13. A semiconductor integrated circuit device according to claim 9, further comprising a regulator circuit, said level shifter converting a lowered potential level signal obtained from the regulator circuit into a power supply voltage level signal to be supplied to an external terminal.

14. A semiconductor integrated circuit device according to claim 13, wherein a transistor included in the level shifter and a device directly receiving the lowered potential level signal is the transistor having the thinnest gate insulation film.

21. A semiconductor integrated circuit device comprising:

a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed; and

an input/output terminal formed on the semiconductor substrate, wherein a transistor connected directly to the input/output terminal, absent any intervening elements, is one of the transistors other than a transistor having the thinnest gate insulation film.

22. A semiconductor integrated circuit device according to claim 21, further comprising a power supply terminal to which an external power supply voltage is applied, wherein a transistor

connected directly to the power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

23. A semiconductor integrated circuit device according to claim 21, further comprising a power supply terminal to which an external power supply voltage is applied and a ground terminal, wherein a transistor having a current path connected between the power supply terminal and the ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

24. A semiconductor integrated circuit device according to claim 21, further comprising an interface circuit connected to the input/output terminal, wherein a transistor included in the interface circuit and connected directly to the input/output terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

25. A semiconductor integrated circuit device according to claim 24, wherein a transistor included in the interface circuit and connected directly to a power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

26. A semiconductor integrated circuit device according to claim 25, wherein a transistor included in the interface circuit and having a current path connected between the power supply

terminal and a ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

27. A semiconductor integrated circuit device according to claim 24, wherein said interface circuit includes an input buffer circuit.

28. A semiconductor integrated circuit device according to claim 24, wherein said interface circuit includes an output buffer circuit.

29. A semiconductor integrated circuit device according to claim 24, wherein said interface circuit includes a level shifter and an output buffer circuit.

30. A semiconductor integrated circuit device according to claim 29, further comprising a regulator circuit, said level shifter converting a lowered potential level signal obtained from the regulator circuit into a power supply voltage level signal to be supplied to an external terminal.

31. A semiconductor integrated circuit device according to claim 30, wherein a transistor included in the level shifter and a device directly receiving the lowered potential level signal is the transistor having the thinnest gate insulation film.

32. A semiconductor integrated circuit device comprising:
a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed; and
an input/output terminal formed on the semiconductor substrate, wherein a transistor always connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film.
33. A semiconductor integrated circuit device according to claim 32, further comprising a power supply terminal to which an external power supply voltage is applied, wherein a transistor connected directly to the power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.
34. A semiconductor integrated circuit device according to claim 32, further comprising a power supply terminal to which an external power supply voltage is applied and a ground terminal, wherein a transistor having a current path connected between the power supply terminal and the ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.
35. A semiconductor integrated circuit device according to claim 32, further comprising an interface circuit connected to the input/output terminal, wherein a transistor included in the

interface circuit and connected directly to the input/output terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

36. A semiconductor integrated circuit device according to claim 35, wherein a transistor included in the interface circuit and connected directly to a power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

37. A semiconductor integrated circuit device according to claim 36, wherein a transistor included in the interface circuit and having a current path connected between the power supply terminal and a ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

38. A semiconductor integrated circuit device according to claim 35, wherein said interface circuit includes an input buffer circuit.

39. A semiconductor integrated circuit device according to claim 35, wherein said interface circuit includes an output buffer circuit.

40. A semiconductor integrated circuit device according to claim 35, wherein said interface circuit includes a level shifter and an output buffer circuit.

41. A semiconductor integrated circuit device according to claim 40, further comprising a regulator circuit, said level shifter converting a lowered potential level signal obtained from the regulator circuit into a power supply voltage level signal to be supplied to an external terminal.

42. A semiconductor integrated circuit device according to claim 41, wherein a transistor included in the level shifter and a device directly receiving the lowered potential level signal is the transistor having the thinnest gate insulation film.